TEXAS INSTRUMENTS

F Logic (SN54/74F)

Data Book

1994

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INTRODUCTION

In this volume, Texas Instruments presents technical information on the SN54/74F TTL logic family. The combination of the SN54/74F family with other Texas Instruments advanced families of TTL integrated circuits, Advanced Low-Power Schottky† (ALS) and Advances Schottky (AS), offers the industry the broadest spectrum of advanced bipolar logic products available from any supplier. In addition, the SN54/74F TTL logic family provides the system designer with a pin-for-pin compatible alternate source for SN54/74F devices in standard 300-mil plastic dual-in-line packages (DIPs) along with plastic small-outline (SO) packages, ceramic chip carriers, and ceramic DIPs. Texas Instruments offers all of the above packages with the service levels, quality, and reliability that users have come to expect in a logic family.

The SN54/74F TTL data sheets have been configured for ease of use. They stand alone and require a minimum of reference to other sections for supporting information. Each data sheet has complete absolute maximum ratings, recommended operating conditions, timing requirements (if applicable), and electrical characteristics. The input/output loading and fanout characteristics of each circuit are specified in terms of actual load-current value in amperes. Pinouts are specified using Texas Instruments TTL name conventions.

The following definitions are for the system design engineer who prefers to use unit loads. One unit load in the high state is defined to be 20 µA. One unit load in the low state is defined to be 0.6 mA.

Logic symbols prepared in accordance with IEEE and IEC standards, logic diagrams, and pinout assignments are provided for all SN54/74F TTL devices. The logic diagrams are provided for the understanding of the logic operation of the device and should not be used to estimate propagation delays. Package dimensions given in the mechanical data section of this book are, with one exception, in inches with metric measurements in parentheses. This is to simplify board layout for designers involved in metric conversion and new designs.

In addition to providing pin-compatible alternate sources to common SN54/74F devices, Texas Instruments has also expanded the family to include new functions and packages. With these new solutions, the system designer has attractive options for new designs and/or upgrades to existing designs.

The SN54/74F240, '244, '245, '373, '374, and '543 functions are now available in standard packages and fine-pitch, EIAJ standard shrink small-outline packages (SSOP) with 0.65-mm pitch for board-area-conscious designs.

The Texas Instruments SN54/74F TTL logic family offers several new logic devices. Included among the new functions are:

'F520	8-bit identity comparator with input pullup resistors and open-collector outputs
'F621	Open-collector octal bus transceiver
'F1056	8-bit enhanced single diode bus-termination array

All devices offered can be characterized into distinct logic functions that address several different applications areas. The following functional group table summarizes these groups and lists specific application areas that the functions address.

Complete technical data for any TI Advanced System Logic product is available from the nearest TI field sales office, local authorized TI distributor, or directly by calling the Advanced System Logic hotline at (214) 997-5202.

FUNCTIONAL GROUPS

FUNCTION	APPLICATIONS
Binary/Decade Counters	Synchronous dividers and multipliers
	Timing circuits and state-machine sequencers
	Pulse and sync generation
	Code-conversion circuits
	Analog-to-digital and digital-to-analog conversion circuits
	Modulo-n event counters and rate multipliers
Decoders	Memory, board, processor, and component-enable generation
	Minterm generation and data-flow control
	Clock-phase splitter and decoder trees
	Demultiplexing for clock distribution and scanning switch encoders
	Program counters and digital display systems
Dual Flip-Flops	Extra register bits (e.g., guard bits and carry bits)
	Synchronizing asynchronous inputs, interrupts, and control signals
	Finite or algorithmic state machine state bits
	Customized modulo-n event counters
Gates	Combinational logic
Identity Comparators	Peripheral and board enables, address decodes, and cache-tag comparisons
	Page-memory boundary detection, page-fault detection, and error detection and correction
Multiplexers/Demultiplexers	Implementing combinational logic (function) tables
	Data-flow-control and parallel-to-serial converters
	Multiplexing trees, asynchronous shifting, and sorting
Octal Buffers/Transceivers	Error-detection and correction circuits
	Hamming code generation
Octal Flip-Flops	Bus-interface, pipeline registers, and customized shift registers
	Ring counters, Johnson counters, pattern generators, and custom modulo-n event counters
	Synchronizing asynchronous inputs, interrupts, and control signals
Shifters/Shift Registers	Serial-to-parallel conversion or parallel-to-serial conversion
	Clock-phase generation, custom counters, and random-number generators
	Pipeline registers, accumulators, and digital filters
	On-board diagnostics and multiply and divide by 2^n
	CPU design and array processors

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